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CLAIMS

1. A process of forming an encapsulated circuit board arrangement having at least one layer of tracks, the encapsulated circuit board arrangement having a first side as an interface side and a second side as a protective cover, wherein the process comprises the steps of:

- applying at least one layer of sequentially processed tracks on a first side of an interface carrier, a second side of the interface carrier being the interface side of the encapsulated circuit board arrangement,
- joining the last applied sequentially processed layer to a support carrier by means of an adhesive layer, the support carrier forming the protective cover of the second side of the encapsulated circuit board arrangement.

2. The process according to claim 1, wherein the process further comprises the step of:

- applying the adhesive layer on top of the last applied sequentially processed layer.

3. The process according to claim 1, wherein the process further comprises the step of:

- applying the adhesive layer to the support carrier.

4. The process according to any one of claims 1 to 3, wherein the application of at least one of the at least one sequentially processed layer is by means of offset printing technology.

5. The process according to claim 4, wherein the step of applying at least one layer of sequentially processed tracks comprises applying an acrylate as a dielectric of at least one of the at least one sequentially processed layer.

6. The process according to any one of claims 2 or 3, wherein the application of the adhesive layer is by means of offset printing technology.

7. The process according to claim 1, wherein the step of joining the last applied sequentially processed layer to a support carrier comprises joining the last applied sequentially processed layer to a support carrier which is at least a part of a cover housing in which the encapsulated circuit board arrangement is mounted.

8. The process according to claim 1, wherein the step of joining the last applied sequentially processed layer to a support carrier comprises joining the last applied sequentially processed layer to a support carrier which is at least a part of an enclosure on which the encapsulated circuit board arrangement is mounted.

9. The process according to claim 1, wherein the step of joining the last applied sequentially processed layer to a support carrier comprises joining the last applied sequentially processed layer to a support carrier which is rigid.

10. The process according to claim 1, wherein the step of joining the last applied sequentially processed layer to a support carrier comprises joining the last applied sequentially processed layer to a support carrier which is bendable.

11. The process according to claim 1, wherein the step of applying at least one layer of sequentially processed tracks comprises applying at least one sequentially processed layer comprising connection circuitry.

12. The process according to any one of claims 1 or 11, wherein the step of applying at least one layer of sequentially processed tracks comprises applying at least one sequentially processed layer comprising tracks arranged as at least one passive component.

13. The process according to any one of claims 1, 11 or 12, wherein the step of applying at least one layer of sequentially processed tracks comprises applying at least one sequentially processed layer comprising tracks arranged as at least one active component.

14. The process according to claim 1, wherein the step of applying at least one layer of sequentially processed tracks comprises applying the at least one layer to an interface layer comprising at least one via.

15. The process according to claim 1, wherein the step of applying at least one layer of sequentially processed tracks comprises applying the at least one layer to an interface layer comprising at least one solid via.

16. The process according to any one of claims 1, 14 or 15, wherein the step of applying at least one layer of sequentially processed tracks comprises applying the at least one layer to an interface layer which is bendable.

17. The process according to any one of claims 1 or 16, wherein the step of applying at least one layer of sequentially processed tracks comprises applying the at least one layer to an interface layer which is made of polymide.

18. A device comprising wireless communication means, wherein the device comprises an encapsulated circuit board arrangement made according any one of claims 1 to 17.

19. A wireless mobile terminal, wherein the terminal comprises an encapsulated circuit board arrangement made according any one of claims 1 to 17.

20. An encapsulated circuit board arrangement having at least one sequentially processed track layer, the encapsulated circuit board arrangement having a first side as an interface side and a second side as a protective cover, wherein the circuit board arrangement comprises:

- an interface layer having a first side and a second side, a first side of the interface layer being the interface side of the encapsulated circuit,
- at least one layer of sequentially processed trackson the second side of the interface carrier,
- a support carrier forming the protective cover of the second side of the encapsulated circuit board arrangement,
- an adhesive layer between a top of the last sequentially processed layer and the support carrier.

21. The circuit board arrangement according to claim 20, wherein at least one of the at least one sequentially processed layer has been added by means of offset printing technology.

22. The circuit board arrangement according to claim 21, wherein a dielectric of at least one of the at least one sequentially processed layer is acrylate.

23. The circuit board arrangement according to any one of claims 20 to 22, wherein the adhesive layer has been added by means of offset printing technology.

24. The circuit board arrangement according to any one of claims 20 to 22, wherein the support carrier is at least a part of a cover housing in which the encapsulated circuit is mounted.

25. The circuit board arrangement according to any one of claims 20 to 22, wherein the support carrier is at least a part of an enclosure on which the encapsulated circuit board arrangement is mounted.

26. The circuit board arrangement according to any one of claims 20 to 22, wherein the support carrier is rigid.

27. The circuit board arrangement according to any one of claims 20 to 22, wherein the support carrier is bendable.

28. The circuit board arrangement according to claim 20, wherein at least one of the at least one sequentially processed layer comprises connection circuitry.

29. The circuit board arrangement according to any one of claims 20 or 28, wherein at least one of the at least one sequentially processed layer comprises tracks arranged as at least one passive component.

30. The circuit board arrangement according to any one of claims 20, 28 or 29, wherein at least one of the at least one sequentially processed layer comprises tracks arranged as at least one active component.

31. The circuit board arrangement according to 20, wherein the interface layer comprises at least one via.

32. The circuit board arrangement according to claim 31, wherein at least one of the at least one via is solid.

33. The circuit board arrangement according to any one of claims 20, 31 or 32, wherein the interface layer is bendable.

34. The circuit board arrangement according to any one of claims 20 or 32, wherein the interface layer is made of polymide.

35. A device comprising wireless communication means, wherein the device comprises an encapsulated circuit board arrangement according any one of claims 20 to 34.

36. A wireless mobile terminal, wherein the terminal comprises an encapsulated circuit board arrangement according any one of claims 20 to 34.